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In re Application

Inventor(s): OM P. AGRAWAL et al.

SC/Serial No.: 09/235,615

Filed: January 21, 1999

Title: FPGA INTEGRATED CIRCUIT HAVING EMBEDDED)

SRAM MEMORY BLOCKS WITH REGISTERED

ADDRESS AND DATA INPUT SECTIONS

) PATENT APPLICATION

)

) Art Unit: 2819

) Examiner:

)

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8  
I hereby certify that this correspondence is being deposited in the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Assistant Commissioner for Patents, Washington, D.C. 20231, on March 20, 2000.

  
Gideon Gimlan, Reg. No. 31,955  
Signature Date: March 20, 2000

(Attorney Signature)

Assistant Commissioner for Patents  
Washington, D.C. 20231

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Sir:

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It is requested that the information identified in this statement be considered by the Examiner and made of record in the above-identified application. This statement is not intended to represent that a search has been made or that the information cited in the statement is, or is considered to be, material to patentability as defined in 37 C.F.R. §1.56.

***Enclosed with this statement are the following:***

- Form PTO-1449. The Examiner is requested to initial the form and return it to the undersigned in accordance with M.P.E.P. §609.
- A copy of each cited document as required by 37 C.F.R. §1.98. Copies are not submitted of U.S. applications, 37 C.F.R. §1.98(a)(2)(iii), and copies are not submitted of documents already cited or submitted in a parent application from which benefit under 35 U.S.C. §120 is claimed, 37 C.F.R. §1.98(d). If any of the cited/submitted documents is in a foreign language, a concise explanation of relevancy is provided pursuant to 37 C.F.R. §1.98(a)(3). For foreign language documents cited in a search report by a foreign patent office, the requirement for a concise explanation of relevance is satisfied by the submission herewith of an English language version of the search report. MPEP §609A(3). If a written English-language translation of a non-English language document, or portion thereof, is within the possession, custody or control of, or is readily available to any individual designated in §1.56(c), a copy of the translation accompanies this statement. 37 C.F.R. §1.98(c).

**This statement should be considered because:**

This statement qualifies under 37 C.F.R. §1.97, subsection (b) because:

- (1) It is being filed within 3 months of the application filing date;  
-- OR --
- (2) It is being filed within 3 months of entry of a national stage;  
-- OR --
- (3) It is being filed before the mailing date of the first Office action on the merits,  
whichever occurs last.

Although it may not qualify under subsection (b), this statement qualifies under 37 C.F.R. §1.97, subsection (c) because:

- (1) It is being filed before the mailing date of a FINAL Office Action and before a Notice of Allowance (whichever occurs first)

-- AND (check at least one of the following) --

- (1) It is accompanied by the \$240 fee set forth in 37 C.F.R. §1.17(p)  
-- OR --
- (2) It is accompanied by a STATEMENT as set forth in 37 C.F.R. §1.97(e)

Although it may not qualify under subsection (b) or (c), this statement qualifies under 37 C.F.R. §1.97, subsection (d) because:

- (1) It is accompanied by a STATEMENT as set forth in 37 C.F.R. §1.97(e);  
-- AND --
- (2) It is accompanied by a PETITION TO ACCEPT INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §1.97(d);  
-- AND --
- (3) It is accompanied by the \$130 fee set forth in 37 C.F.R. §1.17(i)(1);  
-- AND --
- (4) The Issue Fee has not yet been paid.

**Fee Authorization.** The Commissioner is hereby authorized to charge underpayment of any additional fees or credit any overpayment associated with this communication to Deposit Account No. 06-1325. A duplicate copy of this authorization is enclosed.

Respectfully submitted,

FLIESLER, DUBB, MEYER & LOVEJOY LLP

Date: 3-20-2000

By: G.D.  
Gideon Gimlan  
Reg. No. 31,955

## REMARKS

The following Remarks are supplied as part of or in supplement to this Information Disclosure Statement.

In the Abstract of Young application WO 98/10517, "dedicated" address and data lines are said to access the RAM blocks and are stated as being connectable to the general interconnect structure. The term "dedicated" is afterwards applied to vertical lines that are said to carry control as well as address and data signals.

Fig. 2 shows details of a single "RAM block". This RAM block, which is also shown coarsely in Fig. 1B, has four general interconnect, horizontal buses L0-L3 passing through a bottom portion of the block. Each of buses L0-L3 corresponds to a "row" of logic blocks. The latter feature is best seen in Fig. 8A where rows of adjacent logic blocks such as 25-26 and 25-28 are shown.

The RAM module 131 at the top of Fig. 2 is straddled by the "dedicated" vertical lines. Signal inputting ones of the vertical lines are shown to the left of RAM module 131 while signal outputting lines are shown to the right. Except for the four global clock lines (GCLK) at the extreme left of Fig. 2, all other dedicated vertical lines are "programmably" connectable to similar vertical lines of a next-higher RAM block (see page 6, line 35). The latter feature is best seen in Fig. 6A where darkened circles represent programmable connections that are closed while clear circles represent programmable connections that are left open (page 15, lines 24-32).

In Fig. 2, the programmable connections of the data output buses (DOUTB, DOUTA) are represented by the hollow circles at the top, which circles are indicated to be unbuffered programmable data connections (page 8, line 30) or pass transistors (page 4, line 38).

By contrast, the "programmable connections" for the left-side vertical dedicated lines of Fig. 2 are represented by special "pentagon" symbols. The symbol is best seen in Fig. 4A. Horizontal line C is an input into the RAM module 131 while the vertical lines, A and B, represent programmably-splittable parts of a dedicated vertical line. When memory cells M1 and M2 are both 0, high impedance separations are formed between each of lines A, B and the interior of the pentagon-shaped, "bidirectional buffer" (page 9, line 32). When the M1/M2 state is 10, then the data flow direction is from top to bottom (from B to A) with a buffered copy of the signal being presented to horizontal line C. Signal buffering is performed by "buffer element" 41. When the M1/M2 state is instead 01, signal flow is in the bottom-up direction (from A to B). The circle/triangle symbol shown at the extreme left of Fig. 4B represents the same circuit. This circle/triangle symbology appears in Fig. 7B.

Although diamond-shaped connections are shown between the L0-L3 buses and the dedicated vertical lines, the specification speaks of them as being "circles" at page 10, line 31, and also at page 11, line 11. Presumably, these circles correspond to the PIP symbol shown in Fig. 3A.

Two specific embodiments are described in the specification and respectively represented at the gross level by Fig. 1B and Fig. 1C. One difference is that the second embodiment of Fig. 1C does not include a block-enable control (page 6, line 36). Another feature is that the Fig. 1C embodiment has "staggered" line rotation between adjacent

RAM blocks (page 7, line 12). Yet another feature of the Fig. 1C embodiment, which is shown only in Fig. 7A, is that "longer" horizontal lines such as HL0-HL3 also pass through the RAM blocks (page 18, line 21).

Decoders 132 of Fig. 2 are shown in detail in Fig. 5. These can be used for expanding the address space when RAM blocks are "programmably" joined together.

Respectfully submitted,

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Date: 3-20-2000

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